ABSTRACT

This invention reduces redundant power consumption by early detection of predicate register values. This detects pending writes to the predicate registers. When there are no pending predicate register updates, the predicate value is read in the decode stage and a decision whether to nullify the instruction is made. When a write is pending, the instruction executes normally and the result write-back only is dependent upon the newly written predicate value. In the former case, nullifying an instruction completion saves power. The compiler attempts to increase the distance between the predicate-definition and predicate-use by the number of cycles required by the architecture. This scheduling increases the conditions under which the early predicate detection is possible and hence enhances the possibility of power saving.